AMENDMENT TO THE CLAIMS

This Listing of Claims will replace all prior versions, listing, of claims in the specification.

LISTING OF CLAIMS:

Claim 1 (original) A transistor, comprising,

a first conducting structure upon a substrate;

a second conducting structure upon said substrate, with the projection of said second conducting structure onto said substrate intersecting the projection of said first conducting structure onto said substrate;

a third conducting structure upon said substrate contacting with said first conducting structure, with the projection of said third conducting structure onto said substrate separated from said projection of said second conducting structure onto said substrate;

a fourth conducting structure upon said substrate contacting with said second conducting structure, with the projection of said fourth conducting structure onto said substrate separated from said projection of said first conducting structure onto said substrate, and said fourth conducting structure onto said substrate intersecting the projection of said third conducting structure onto said substrate; and

a fifth conducting structure upon said substrate, with the projection of said fifth conducting structure onto said substrate at least partly overlapping said projection of said fourth conducting structure onto said substrate and separated from said projection of said third, said first, and said second conducting structure onto said substrate.

Claim 2 (original) The transistor as set forth in Claim 1, wherein said projection of said fifth and said second conducting structure onto said substrate being on the opposite sides of said projection of said third conducting structure onto said substrate.

Claim 3 (original) The transistor as set forth in Claim 1, wherein said projection of said fifth conducting structure onto said substrate not contacting with the end of said projection of said fourth conducting structure onto said substrate not contacting with said second conducting structure.

Claim 4 (original) The transistor as set forth in Claim 1, wherein said projection of said fifth conducting structure onto said substrate completely inside said projection of said fourth conducting structure onto said substrate.

Claim 5 (original) The transistor as set forth in Claim 1, while said projection of said fifth conducting structure onto said substrate not completely inside said projection of said fourth conducting structure onto said substrate, said projection of said fifth conducting structure onto said substrate not contacting with the end of said projection of said fourth conducting structure onto said substrate not contacting with said second conducting structure.

Claim 6 (original) The transistor as set forth in Claim 5, wherein the opposite two sides of said projection of said fourth conducting structure onto said substrate passed by said projection of said fifth conducting structure onto said substrate approximately parallel to one another at and near the intersecting area of said projection of said fourth and said fifth conducting structure.

Claim 7 (original) The transistor as set forth in Claim 1, wherein the opposite two sides of said projection of said fifth conducting structure onto said substrate passed by said projection of said fourth conducting structure onto said substrate approximately parallel to one another at and near the intersecting area of said projection of said fourth and said fifth conducting structure.

Claim 8 (original) The transistor as set forth in Claim 1, wherein said projection of said fifth and said fourth conducting structure onto said substrate being approximately parallelograms.

Claim 9 (original) The transistor as set forth in Claim 1, further comprising a semiconductor layer upon said substrate and electrically coupling with said third and said fifth conducting structure with the projection of said semiconductor layer onto said substrate completely inside said projection of said fourth conducting structure onto said substrate.

Claim 10 (original) A transistor, comprising,

a first conducting structure upon a substrate;

a second conducting structure upon said substrate, with the projection of said second conducting structure onto said substrate intersecting the projection of said first conducting structure onto said substrate;

a third conducting structure upon said substrate contacting with said first conducting structure, with the projection of said third conducting structure onto said substrate completely inside said projection of said second conducting structure onto said substrate; and

a fourth conducting structure upon said substrate, with the projection of said fourth conducting structure onto said substrate separated from said projection of said first and said third conducting structure onto said substrate, said projection

of said fourth conducting structure onto said substrate completely inside said projection of said second conducting structure onto said substrate; and said projection of said fourth conducting structure onto said substrate approximately parallel to said projection of said third conducting structure onto said substrate.

Claim 11 (original) The transistor as set forth in Claim 10, wherein the side of said projection of said fourth conducting structure onto said substrate approximately parallel to said projection of said third conducting structure onto said substrate far longer than the side of said projection of said fourth conducting structure onto said substrate approximately parallel to said projection of said first conducting structure onto said substrate.

Claim 12 (original) The transistor as set forth in Claim 10, wherein said side of said projection of said fourth conducting structure onto said substrate approximately parallel to said projection of said third conducting structure onto said substrate at least seven times longer than said side of said projection of said fourth conducting structure onto said substrate approximately parallel to said projection of said first conducting structure onto said substrate.

Claim 13 (original) The transistor as set forth in Claim 10, further comprising a fifth conducting structure upon said substrate contacting with said fourth conducting structure, with the projection of said fifth conducting structure onto said substrate separated from said projection of said first and said third conducting structure onto said substrate, said projection of said fifth conducting structure onto said substrate at least partly inside said projection of said second conducting structure onto said substrate, said projection of said fifth and said third conducting structure onto said substrate on the opposite sides of said projection of said fourth conducting structure onto said substrate, and the side of said projection

of said fourth conducting structure onto said substrate facing said projection of said fifth conducting structure onto said substrate only partly contacting with said projection of said fifth conducting structure onto said substrate.

Claim 14 (original) The transistor as set forth in Claim 13, wherein the area of said projection of said fourth conducting structure onto said substrate far larger than that of the overlap between said projection of said fifth and said second conducting structure.

Claim 15 (original) The transistor as set forth in Claim 10, further comprising a semiconductor layer upon said substrate electrically coupling with said third and said fourth conducting structure, with the projection of said semiconductor layer onto said substrate completely inside said projection of said second conducting structure onto said substrate.

Claims 16-20 (canceled).